

PFE1100-12-054xA

Front-End AC-DC Power Supply

The PFE1100-12-054xA is a 1100 Watt AC to DC power-factor-corrected (PFC) power supply that converts standard AC mains power into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PFE1100-12-054xA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



Key Features & Benefits

- Best-in-class, 80 PLUS certified “Platinum” efficiency
- Wide input voltage range: 90-264 VAC
- AC input with power factor correction
- Always-On 16.5 W programmable standby output (3.3/5 V)
- Hot-plug capable
- Parallel operation with active digital current sharing
- Full digital controls for improved performance
- High density design: 25.6 W/in³
- Small form factor: 321.5 x 54.5 x 40 mm (12.66 x 2.14 x 1.57 in)
- I²C communication interface for control, programming and monitoring with PSMI and Power Management Bus protocol
- Overtemperature, output overvoltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: AC OK and DC OK with fault signaling

Applications

- High Performance Servers
- Routers
- Switches



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1. ORDERING INFORMATION

| PFE | 1100 | - | 12 | - | 054 | x | A |
|----------------|-------------|------|-----------|------|-------|-------------------------|-------|
| Product Family | Power Level | Dash | V1 Output | Dash | Width | Airflow | Input |
| PFE Front-Ends | 1100 W | | 12 V | | 54 mm | N: Normal R: Reverse | A: AC |

2. OVERVIEW

The PFE1100-12-054xA AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal linear derating of output power with input voltage and temperature, the PFE1100-12-054xA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths. The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output, with selectable voltage level (3.3/5.0 Volts), provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability. Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

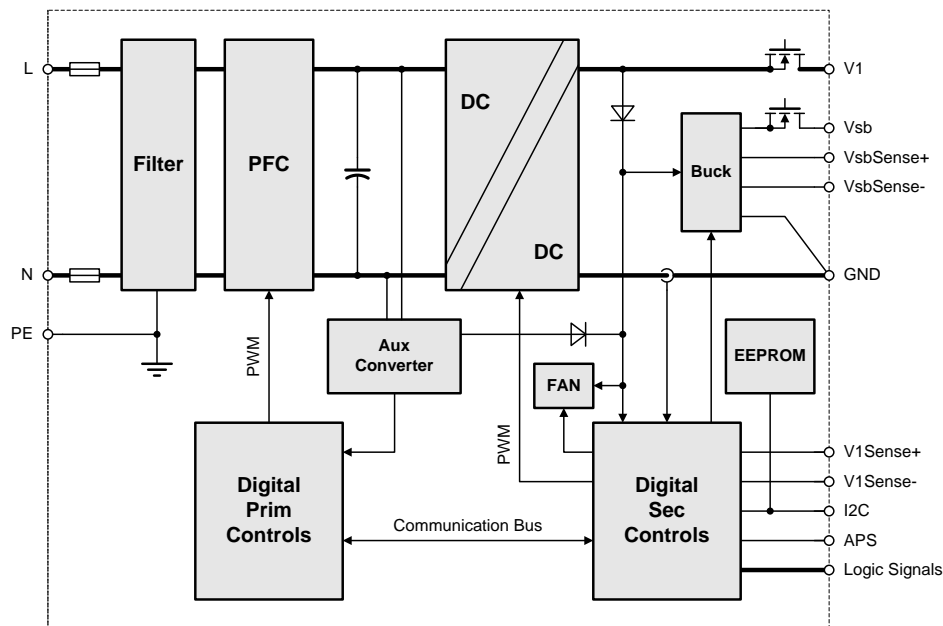


Figure 1. PFE1100-12-054xA Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the supply.

| PARAMETER | CONDITIONS / DESCRIPTION | MIN | MAX | UNITS |
|-------------|--------------------------|-----|-----|-------|
| $V_i\ maxc$ | Maximum Input | | 264 | VAC |



4. INPUT

General Condition: $T_A = 0 \dots 45 \text{ }^\circ\text{C}$ unless otherwise noted.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNITS |
|-------------------|-------------------------------------|---|-------|------|------------------|
| $V_{i\text{nom}}$ | Nominal Input Voltage | 100 | 230 | 230 | VAC |
| V_i | Input Voltage Ranges | Normal operating ($V_{i\text{min}}$ to $V_{i\text{max}}$) | | 264 | VAC |
| $V_{i\text{red}}$ | Derated Input Voltage Range | See Figure 20 and Figure 40 | | 180 | VAC |
| $I_{i\text{max}}$ | Max Input Current | | | 13 | A _{rms} |
| $I_{i\text{p}}$ | Inrush Current Limitation | $V_{i\text{min}}$ to $V_{i\text{max}}$, $\bar{T}_{\text{NTC}} = 25^\circ\text{C}$ (Figure 5) | | 40 | A _p |
| F_i | Input Frequency | 47 | 50/60 | 64 | Hz |
| PF | Power Factor | $V_{i\text{nom}}$, 50Hz, $> 0.3 I_{i\text{nom}}$ | | | W/VA |
| $V_{i\text{on}}$ | Turn-on Input Voltage ¹ | Ramping up | | 87 | VAC |
| $V_{i\text{off}}$ | Turn-off Input Voltage ¹ | Ramping down | | 85 | VAC |
| η | Efficiency without Fan | $V_{i\text{nom}}$, $0.1 \cdot k_{\text{nom}}$, $V_{x\text{nom}}$, $T_A = 25^\circ\text{C}$ | | 90.3 | % |
| | | $V_{i\text{nom}}$, $0.2 \cdot k_{\text{nom}}$, $V_{x\text{nom}}$, $T_A = 25^\circ\text{C}$ | | 93.4 | |
| | | $V_{i\text{nom}}$, $0.5 \cdot k_{\text{nom}}$, $V_{x\text{nom}}$, $T_A = 25^\circ\text{C}$ | | 94.5 | |
| | | $V_{i\text{nom}}$, k_{nom} , $V_{x\text{nom}}$, $T_A = 25^\circ\text{C}$ | | 93.8 | |
| T_{hold} | Hold-up Time | After last AC zero point, $V_i > 10.8\text{V}$, V_{SB} within regulation, $V_i = 230\text{VAC}$, $P_{x\text{nom}}$ | | 12 | ms |

4.1 INPUT FUSE

Quick-acting 16 A input fuses (5 x 20 mm) in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.2 μF , resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

NOTE:

Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input undervoltage lockout threshold $V_{i\text{on}}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

In addition, the PFC circuit has a stability region to be observed when operating the power supply at high input current amplitudes. At a low source inductance (<150 μH) the power supply will work stable up to its full maximum input current (13 Arms). If the source inductance is higher, the region with stable PFC operation is slightly reduced (as shown in [Figure 4](#)). The power supply will also work in the unstable region, but it may exhibit a slight current oscillation during the sinusoidal peak.

¹ The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.



4.5 EFFICIENCY

High efficiency (see *Figure 2*) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

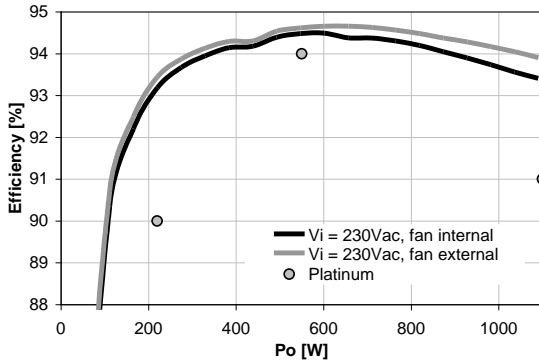


Figure 2. Efficiency vs. Load current (ratio metric loading)

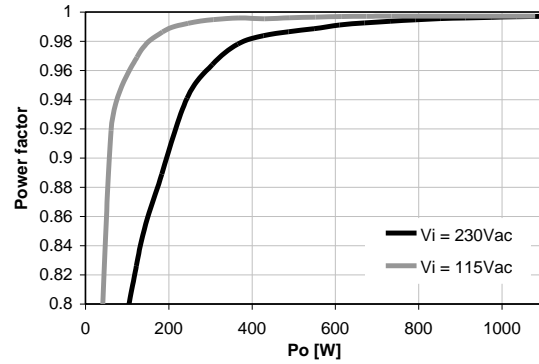


Figure 3. Power factor vs. Load current

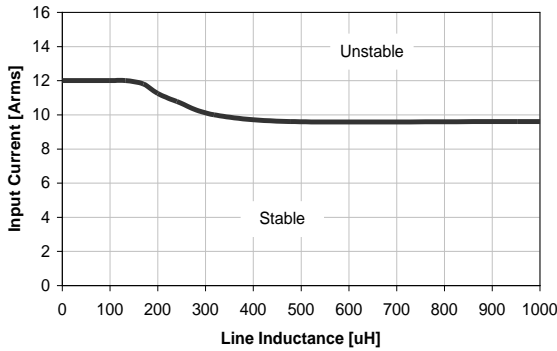


Figure 4. PFC Stability Region

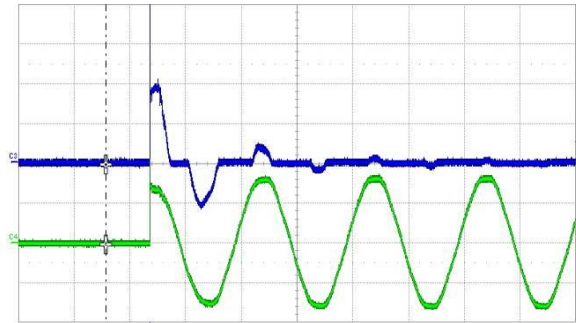


Figure 5. Inrush current, $V_{in} = 230Vac, 90^\circ$
 CH4: V_{in} (200V/div), CH3: I_{in} (20A/div)



5. OUTPUT

General Condition: $T_a = 0 \dots +45 \text{ }^\circ\text{C}$ unless otherwise noted.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--|--------------------------|---|------|-------|-----------------------|
| Main Output V_1 | | | | | |
| $V_1 \text{ nom}$ | Nominal Output Voltage | | 12.0 | | VDC |
| $V_1 \text{ set}$ | Output Setpoint Accuracy | -0.5 | | +0.5 | % $V_1 \text{ nom}$ |
| $dV_1 \text{ tot}$ | Total Regulation | $V_1 \text{ min}$ to $V_1 \text{ max}$, 0 to 100% $I_1 \text{ nom}$, $T_a \text{ min}$ to $T_a \text{ max}$ | | | % $V_1 \text{ nom}$ |
| $P_1 \text{ nom}$ | Nominal Output Power | | 1080 | | W |
| $I_1 \text{ nom}$ | Nominal Output Current | | 90.0 | | ADC |
| $V_1 \text{ pp}$ | Output Ripple Voltage | | | 150 | mVpp |
| $dV_1 \text{ Load}$ | Load Regulation | | 60 | | mV |
| $dV_1 \text{ Line}$ | Line Regulation | | 0 | | mV |
| $I_1 \text{ max}$ | Current Limitation | | 93.5 | 100 | ADC |
| | PFE1100-12-054NA | $V_1 > 115 \text{ VAC}$, $T_a < 45^\circ\text{C}$ | 74 | 78 | |
| | Current Limitation | $V_1 > 90 \text{ VAC}$, $T_a < 45^\circ\text{C}$ | 91 | 95 | |
| | PFE1100-12-054RA | $V_1 > 180 \text{ VAC}$, $T_a < 45^\circ\text{C}$ | 71 | 75 | |
| dI_{share} | Current Sharing | Deviation from $I_1 \text{ tot} / N$, $I_1 > 10\%$ | -3 | +3 | A |
| dV_{dyn} | Dynamic Load Regulation | $\Delta I_1 = 50\% I_1 \text{ nom}$, $I_1 = 5 \dots 100\% I_1 \text{ nom}$, $dI_1/dt = 1\text{A}/\mu\text{s}$, recovery within 1% of $V_1 \text{ nom}$ | -0.6 | 0.6 | V |
| T_{rec} | Recovery Time | | | 1 | ms |
| $t_{\text{AC } V_1}$ | Start-up Time from AC | | | 2 | sec |
| $t_{V_1 \text{ rise}}$ | Rise Time | | 1 | 10 | ms |
| C_{Load} | Capacitive Loading | | | 30000 | μF |
| Standby Output V_{SB} | | | | | |
| $V_{\text{SB}} \text{ nom}$ | Nominal Output Voltage | | 3.3 | | VDC |
| $V_{\text{SB}} \text{ set}$ | Output Setpoint Accuracy | $V_{\text{SB_SEL}} = 1$ | | 5.0 | % $V_{\text{SB nom}}$ |
| | | $V_{\text{SB_SEL}} = 0$ | -0.5 | +0.5 | |
| | | $V_{\text{SB_SEL}} = 0 / 1$ | | | |
| $dV_{\text{SB}} \text{ tot}$ | Total Regulation | $V_{\text{SB}} \text{ min}$ to $V_{\text{SB}} \text{ max}$, 0 to 100% $I_{\text{SB}} \text{ nom}$, $T_a \text{ min}$ to $T_a \text{ max}$ | | | % $V_{\text{SB nom}}$ |
| $P_{\text{SB}} \text{ nom}$ | Nominal Output Power | $V_{\text{SB}} = 3.3 \text{ VDC}$, normal airflow | | 16.5 | W |
| | | $V_{\text{SB}} = 3.3 \text{ VDC}$, reverse airflow | | 11.5 | |
| | | $V_{\text{SB}} = 5.0 \text{ VDC}$, normal/reverse airflow | | 16.5 | |
| $I_{\text{SB}} \text{ nom}$ | Nominal Output Current | $V_{\text{SB}} = 3.3 \text{ VDC}$, normal airflow | | 5 | ADC |
| | | $V_{\text{SB}} = 3.3 \text{ VDC}$, reverse airflow | | 3.5 | |
| | | $V_{\text{SB}} = 5.0 \text{ VDC}$, normal/reverse airflow | | 3.3 | |
| $V_{\text{SB}} \text{ pp}$ | Output Ripple Voltage | | | 100 | mVpp |
| dV_{SB} | Drop | $V_{\text{SB_SEL}} = 1$ | | 67 | mV |
| | | $V_{\text{SB_SEL}} = 0$ | | 44 | |
| $I_{\text{SB}} \text{ max}$ | Current Limitation | $V_{\text{SB_SEL}} = 1$, normal airflow | 5.25 | 6 | ADC |
| | | $V_{\text{SB_SEL}} = 1$, reverse airflow | 4 | 4.75 | |
| | | $V_{\text{SB_SEL}} = 0$, normal/reverse airflow | 3.45 | 4.3 | |
| $dV_{\text{SB}} \text{ dyn}$ | Dynamic Load Regulation | $\Delta I_{\text{SB}} = 50\% I_{\text{SB}} \text{ nom}$, $I_{\text{SB}} = 5 \dots 100\% I_{\text{SB}} \text{ nom}$, $dI_{\text{SB}}/dt = 0.5 \text{ A}/\mu\text{s}$, recovery within 1% of $V_1 \text{ nom}$ | -3 | 3 | % $V_{\text{SB nom}}$ |
| T_{rec} | Recovery Time | | | 250 | μs |
| $t_{\text{AC } V_{\text{SB}}}$ | Start-up Time from AC | | | 2 | sec |
| $t_{V_{\text{SB}} \text{ rise}}$ | Rise Time | | 4 | 20 | ms |
| C_{Load} | Capacitive Loading | | | 10000 | μF |



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5.1 OUTPUT VOLTAGE RIPPLE

Internal capacitance at the 12 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

The setup of *Figure 6* has been used to evaluate suitable capacitor types. The capacitor combinations of *Table 1* and *Table 2* should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

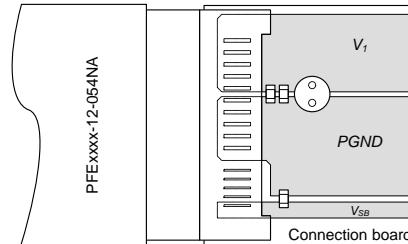


Figure 6. Output ripple test setup

NOTE:

Care must be taken when using ceramic capacitors with a total capacitance of 1 μF to 50 μF on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

| External capacitor V1 | dV1max | Unit |
|--|--------|------|
| 2Pcs 47 $\mu\text{F}/16 \text{ V}/\text{X5R}/1210$ | 150 | mVpp |
| 1Pcs 1000 $\mu\text{F}/16 \text{ V}/\text{Low ESR Aluminum}/\phi 10 \times 20$ | 120 | mVpp |
| 1Pcs 270 $\mu\text{F}/16 \text{ V}/\text{Conductive Polymer}/\phi 8 \times 12$ | 120 | mVpp |
| 2Pcs 47 $\mu\text{F}/16 \text{ V}/\text{X5R}/1210$ plus 1Pcs 270 μF Conductive Polymer OR 1Pcs 1000 μF Low ESR AlCap | 60 | mVpp |

Table 1. Suitable capacitors for V1

| External capacitor VSB | dV1max | Unit |
|--|--------|------|
| 1Pcs 10 $\mu\text{F}/16 \text{ V}/\text{X5R}/1206$ | 80 | mVpp |
| 2Pcs 10 $\mu\text{F}/16 \text{ V}/\text{X5R}/1206$ | 50 | mVpp |
| 1Pcs 47 $\mu\text{F}/16 \text{ V}/\text{X5R}/1210$ | 40 | mVpp |
| 2Pcs 100 $\mu\text{F}/6.3 \text{ V}/\text{X5R}/1206$ | 30 | mVpp |

Table 2. Suitable capacitors for VSB

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

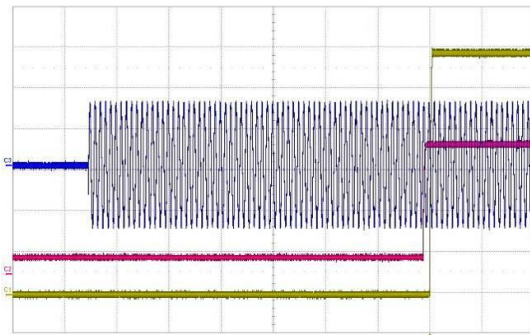


Figure 7. Turn-On AC Line 230VAC, full load (200ms/div)
CH1: V1 (2V/div) CH2: VSB (2V/div) CH3: Vin (200V/div)

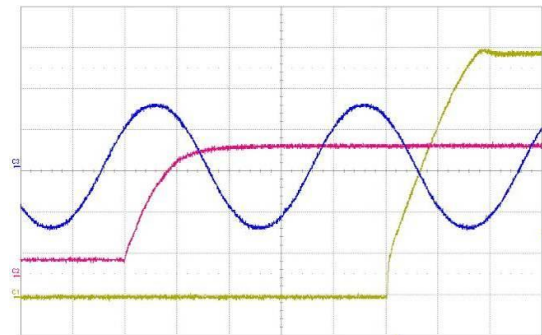


Figure 8. Turn-On AC Line 230VAC, full load (5ms/div)
CH1: V1 (2V/div) CH2: VSB (2V/div) CH3: Vin (200V/div)



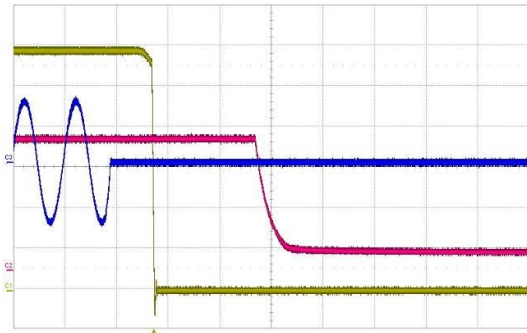


Figure 9. Turn-Off AC Line 230VAC, full load (20ms/div)
 CH1: V₁ (2V/div) CH2: V_{SB} (2V/div) CH3: V_{in} (200V/div)

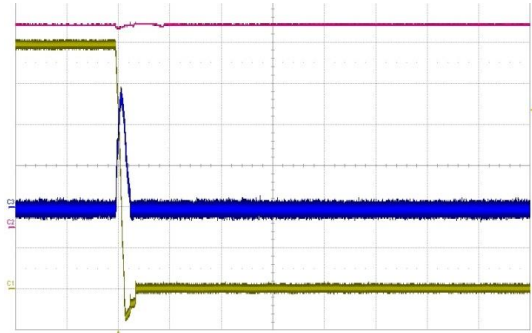


Figure 10. Short circuit on V₁ (500 μs/Div)
 CH1: V₁ (2V/div) CH2: V_{SB} (1V/div) CH3: I₁ (200A/div)

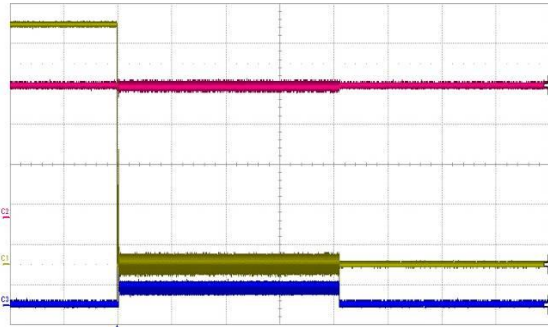


Figure 11. Short circuit on V₁ (50ms/div)
 CH1: V₁ (2V/div) CH2: V_{SB} (1V/div) CH3: I₁ (200A/div)

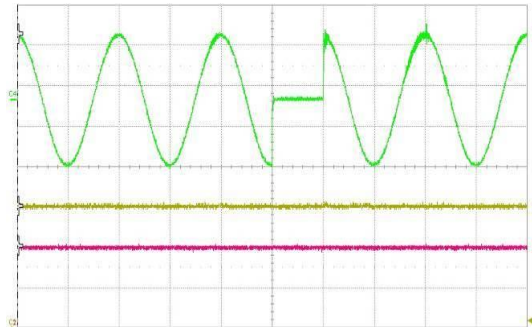


Figure 12. AC drop out 10 ms (10ms/div)
 CH1: V₁ (2V/div) CH2: V_{SB} (1V/div) CH4: V_{in} (200V/div)

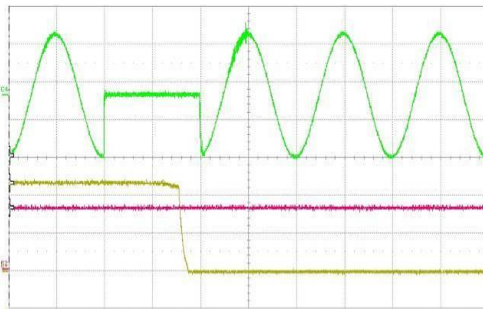


Figure 13. AC drop out 20 ms (10ms/div)
 CH1: V₁ (5V/div) CH2: V_{SB} (2V/div) CH4: V_{in} (200V/div)

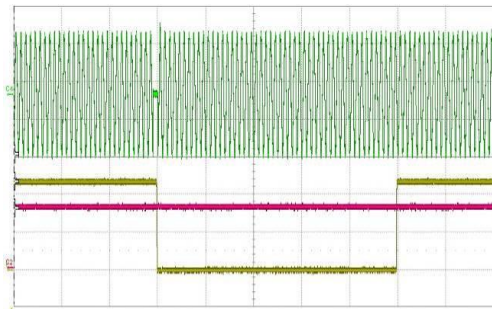


Figure 14. AC drop out 20ms (200ms/div), V₁ restart after 1s
 CH1: V₁ (5V/div) CH2: V_{SB} (2V/div) CH4: I₁ (200V/div)

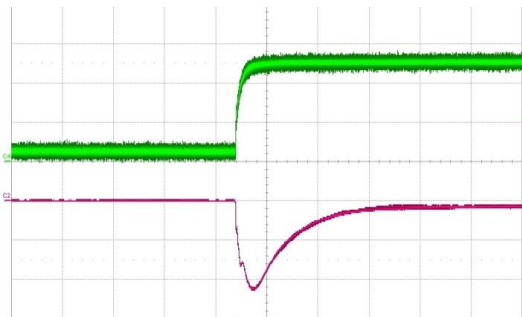


Figure 15. Load transient V₁, 5 to 50A (500 μs/div)
 CH2: V₁ (200mV/div), CH4: I₁ (20A/div)

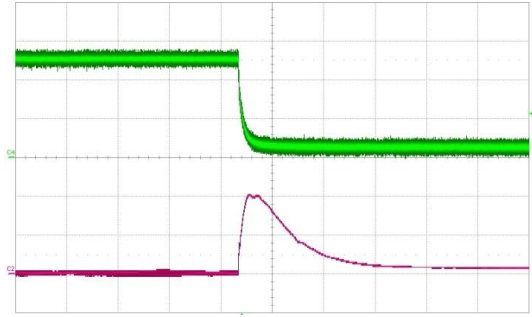


Figure 16. Load transient V₁, 50 to 5A (500 μs/div)
 CH2: V₁ (200mV/div), CH4: I₁ (20A/div)



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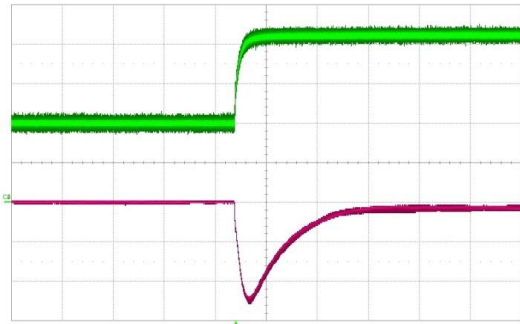


Figure 17. Load transient V_1 , 40 to 85A (500µs/div)
CH2: V_1 (200mV/div), CH4: I_1 (20A/div)

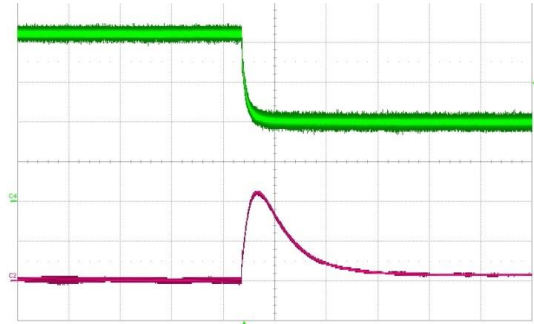


Figure 18. Load transient V_1 , 85 to 40A (500µs/div)
CH2: V_1 (200mV/div), CH4: I_1 (20A/div)

6 PROTECTION

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|-----------------|---------------------------------|--|------|------|------------|
| F | Input Fuses (L+N) | Not user accessible, quick-acting (F) | | 16 | A |
| V_1 ov | OV Threshold V_1 | 13.3 | | 14.5 | VDC |
| $t_{OV V1}$ | OV Latch Off Time V_1 | | | 1 | ms |
| V_{SB} ov | OV Threshold V_{SB} | 115 | | 125 | % V_{SB} |
| $t_{OV VSB}$ | OV Latch Off Time V_{SB} | | | 1 | ms |
| I_1 lim | Current Limit V_1 | $V_1 > 115VAC$, $T_a < 45^\circ C$ | 93.5 | 100 | A |
| | PFE1100-12-054NA | $V_1 > 90VAC$, $T_a < 45^\circ C$ | 74 | 78 | |
| | Current Limit V_1 | $V_1 > 180VAC$, $T_a < 45^\circ C$ | 92 | 100 | |
| | PFE1100-12-054RA | $V_1 > 90VAC$, $T_a < 45^\circ C$ | 72 | 78 | |
| I_1 sc | Max Short Circuit Current I_1 | $V_1 < 3V$ | | 110 | A |
| $t_{I1 sc}$ | Short Circuit Regulation Time | $V_1 < 3V$, time until I_1 is limited to $< I_1$ sc | | 2 | ms |
| $t_{I1 sc off}$ | Short Circuit Latch Off Time | Time to latch off when in short circuit | | 200 | ms |
| T_{SD} | Over Temperature on Heat Sinks | Automatic shut-down | 115 | | $^\circ C$ |

6.1 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.

6.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal if the output voltage exceeds $\pm 5\%$ of its nominal voltage. Output undervoltage protection is provided on the standby output only. When VSB falls below 75% of its nominal voltage, the main output V_1 is inhibited.

6.3 CURRENT LIMITATION

MAIN OUTPUT

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~ 10.0 VDC for more than 200 ms, the output will latch off (standby remains on).



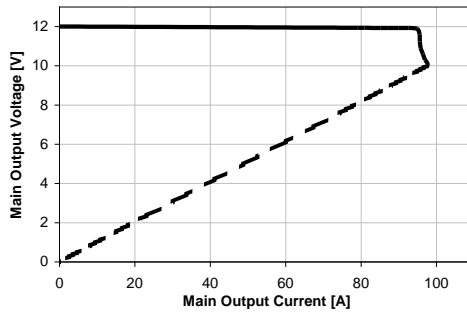


Figure 19. Current Limitation on V_1 ($V_i = 230$ VAC)

A second current limitation circuit on V_1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The supply will re-start 4 ms later with a soft start, if the short circuit persists ($V_1 < 10.0$ V for >200 ms) the output will latch off; otherwise it continuous to operate (hardware current limit triggers).

The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 45°C or if the AC input voltage is too low (see Figure 20 and Figure 21). Note that the actual current limitation on V_1 will begin at a current level approximately 4 A higher than what is shown in Figure 20. (See also Temperature and Fan Control for additional information.)

STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the AC input voltage, but is derated with the ambient temperature (only for reverse airflow).

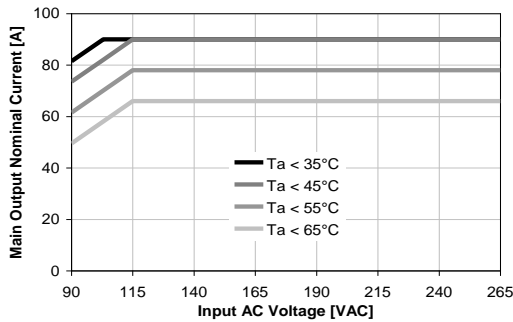


Figure 20. Derating on V_1 vs. V_i and T_a for PFE1100-12-054NA

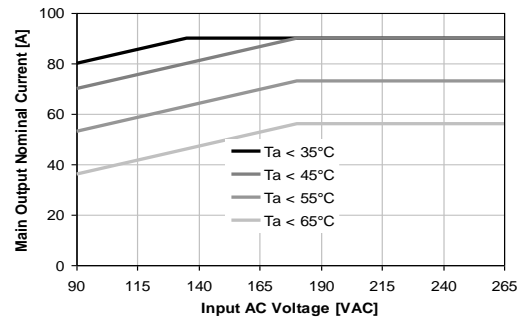


Figure 21. Derating on V_1 vs. V_i and T_a for PFE1100-12-054RA

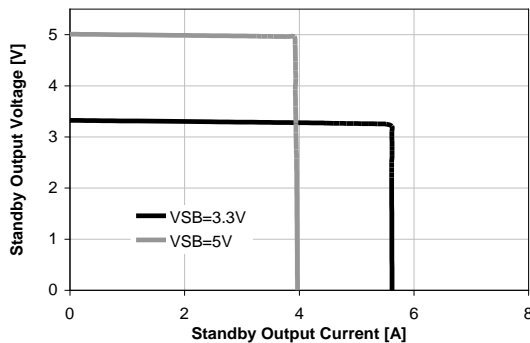


Figure 22. Current limitation on V_{sb}

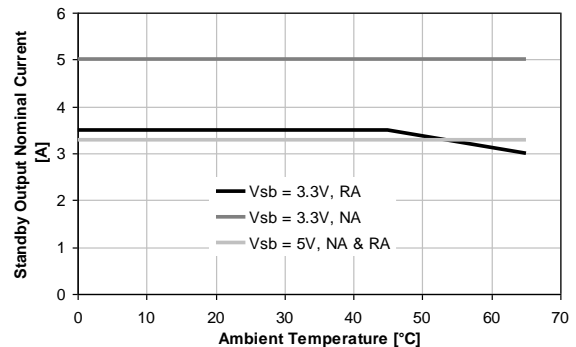


Figure 23. Temperature derating on V_{sb}



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7 MONITORING

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---------------------|--|------|-----|------|------------------|
| $V_{i\text{ mon}}$ | Input RMS Voltage $V_{i\text{ min}} \leq V_i \leq V_{i\text{ max}}$ | -2.5 | | +2.5 | % |
| $I_{i\text{ mon}}$ | Input RMS Current $I_i > 4 A_{\text{rms}}$ $I_i \leq 4 A_{\text{rms}}$ | -5 | | +5 | % |
| | | -0.2 | | +0.2 | A_{rms} |
| $P_{i\text{ mon}}$ | True Input Power $P_i > 100 W$ $P_i \leq 100 W$ | -5 | | +5 | % |
| | | -5 | | +5 | W |
| $V_{1\text{ mon}}$ | V_1 Voltage | -2 | | +2 | % |
| $I_{1\text{ mon}}$ | V_1 Current $I_1 > 10 A$ $I_1 \leq 10 A$ | -2 | | +2 | % |
| | | -0.2 | | +0.2 | A |
| $P_{o\text{ nom}}$ | Total Output Power $P_o > 120 W$ $P_o \leq 120 W$ | -4 | | +4 | % |
| | | -4.5 | | +4.5 | W |
| $V_{SB\text{ mon}}$ | Standby Voltage | -0.1 | | +0.1 | V |
| $I_{SB\text{ mon}}$ | Standby Current $I_{SB} \leq I_{SB\text{ nom}}$ | -0.2 | | +0.2 | A |

8 SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---|---|------|------|-----|---------------|
| <i>PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs</i> | | | | | |
| V_{iL} | Input Low Level Voltage | -0.2 | | 0.8 | V |
| V_{iH} | Input High Level Voltage | 2.4 | | 3.5 | V |
| $I_{iL,H}$ | Maximum Input Sink or Source Current | 0 | | 1 | mA |
| $R_{puPSKILL_H}$ | Internal Pull Up Resistor on PSKILL_H | | 100 | | k Ω |
| R_{puPSON_L} | Internal Pull Up Resistor on PSON_L | | 10 | | k Ω |
| R_{puVSB_SEL} | Internal Pull Up Resistor on VSB_SEL | | 10 | | k Ω |
| $R_{puHOTSTANDBYEN_H}$ | Internal Pull Up Resistor on HOTSTANDBYEN_H | | 10 | | k Ω |
| R_{LOW} | Resistance Pin to SGND for Low Level | 0 | | 1 | k Ω |
| R_{HIGH} | Resistance Pin to SGND for High Level | 50 | | | k Ω |
| <i>PWOK_H Output</i> | | | | | |
| V_{oL} | Output Low Level Voltage $I_{\text{sink}} < 4 \text{ mA}$ | 0 | | 0.4 | V |
| V_{oH} | Output High Level Voltage $I_{\text{source}} < 0.5 \text{ mA}$ | 2.6 | | 3.5 | V |
| R_{puPWOK_H} | Internal Pull Up Resistor on PWOK_H | | 1 | | k Ω |
| <i>ACOK_H Output</i> | | | | | |
| V_{oL} | Output Low Level Voltage $I_{\text{sink}} < 2 \text{ mA}$ | 0 | | 0.4 | V |
| V_{oH} | Output High Level Voltage $I_{\text{source}} < 50 \mu\text{A}$ | 2.6 | | 3.5 | V |
| R_{puACOK_H} | Internal Pull Up Resistor on ACOK_H | | 10 | | k Ω |
| <i>SMB_ALERT_L Output</i> | | | | | |
| V_{ext} | Maximum External Pull Up Voltage | | | 12 | V |
| V_{oL} | Output Low Level Voltage $I_{\text{source}} < 4 \text{ mA}$ | 0 | | 0.4 | V |
| I_{oH} | Maximum High Level Leakage Current | | | 10 | μA |
| $R_{puSMB_ALERT_L}$ | Internal Pull Up Resistor on SMB_ALERT_L | | None | | k Ω |



8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ± 0.5 V. Therefore, all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.

If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in *Figure 24* (Except for SMB_ALERT_L, ISHARE and I²C pins). This will ensure the pin voltage is not affected by an unpowered power supply.

SMB_ALERT_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins.

ISHARE pins must be interconnected without any additional components. This in-/output also has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

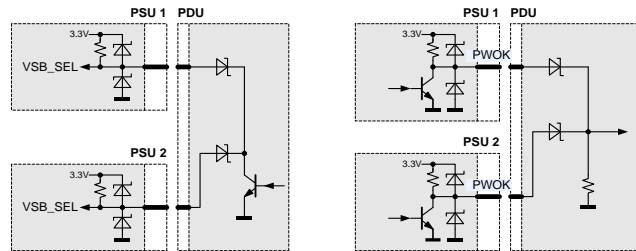


Figure 24. Interconnection of Signal Pins

8.3 FRONT LEDS

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LEDs see Table 1 lists the different LED status.

| OPERATING CONDITION | LED SIGNALING |
|--|-----------------------------|
| AC LED | |
| AC Line within range | Solid Green |
| AC Line UV condition | Off |
| DC LED¹ | |
| PSON_L High | Blinking Yellow (1:1) |
| Hot-Standby Mode | Blinking Yellow/Green (1:2) |
| V_1 or V_{SB} out of regulation | Solid Yellow |
| Over temperature shutdown | |
| Output over voltage shutdown (V_1 or V_{SB}) | |
| Output over current shutdown (V_1 or V_{SB}) | |
| Fan error (>15%) | Blinking Yellow/Green (2:1) |
| Over temperature warning | |
| Minor fan regulation error (>5%, <15%) | |

¹⁾ The order of the criteria in the table corresponds to the testing precedence in the controller.

Table 1. LED Status



8.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10 mA.

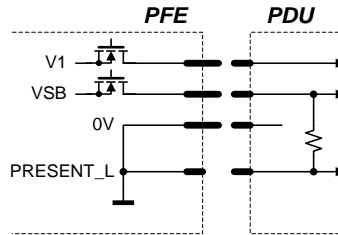


Figure 25. PRESENT_L signal pin

8.5 PSKILL_H INPUT

The PSKILL_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL_H input state.

8.6 AC TURN-ON / DROP-OUTS / ACOK_H

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON_L signal is pulled low and the AC line is within range. The ACOK_H signal is active-high. The timing diagram is shown in Figure 26 and referenced in Table 4.

| OPERATING CONDITION | MIN | MAX | UNIT |
|--|------|------|------|
| $t_{AC\ VSB}$ AC Line to 90% V_{SB} | | 2 | sec |
| $t_{AC\ V1}$ AC Line to 90% V_1 | | 2 | sec |
| $t_{ACOK_H\ on1}$ ACOK_H signal on delay (start-up) | | 2000 | ms |
| $t_{ACOK_H\ on2}$ ACOK_H signal on delay (dips) | | 100 | ms |
| $t_{ACOK_H\ off}$ ACOK_H signal off delay | | 5 | ms |
| $t_{VSB\ V1\ del}$ V_{SB} to V_1 delay | 10 | 500 | ms |
| $t_{V1\ holdup}$ Effective V_1 holdup time | 12 | | ms |
| $t_{VSB\ holdup}$ Effective V_{SB} holdup time | 20 | | ms |
| $t_{ACOK_H\ V1}$ ACOK_H to V_1 holdup | 7 | | ms |
| $t_{ACOK_H\ VSB}$ ACOK_H to V_{SB} holdup | 15 | | ms |
| $t_{V1\ off}$ Minimum V_1 off time | 1000 | 1200 | ms |
| $t_{VSB\ off}$ Minimum V_{SB} off time | 1000 | 1200 | ms |

Table 2. AC Turn-on / Dip Timing

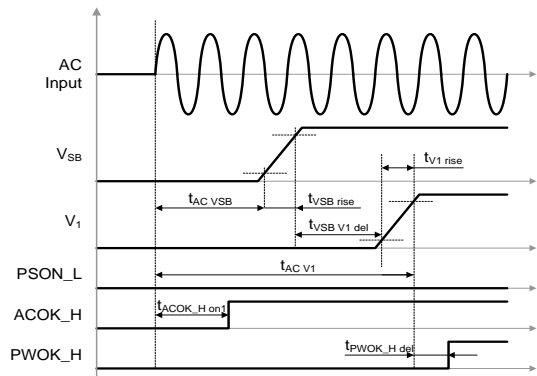


Figure 26. AC turn-on timing



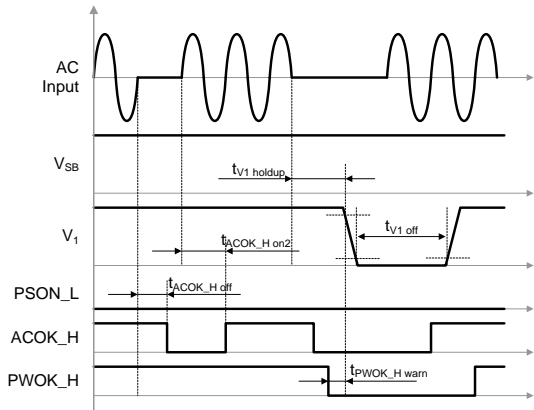


Figure 27. AC short dips

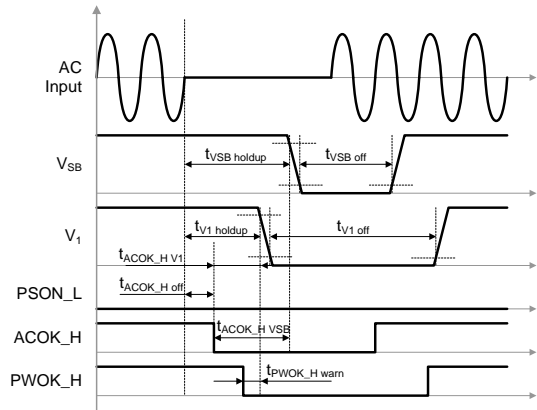


Figure 28. AC long dips

8.7 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given [Figure 29](#) and the parameters in [Table 5](#).

| OPERATING CONDITION | | MIN | MAX | UNIT |
|----------------------------|--------------------------|-----|-----|------|
| $t_{\text{PSON_L V1on}}$ | PSON_L to V1 delay (on) | 2 | 20 | ms |
| $t_{\text{PSON_L V1off}}$ | PSON_L to V1 delay (off) | 2 | 20 | ms |
| $t_{\text{PSON_L H min}}$ | PSON_L minimum High time | 10 | | ms |

Table 3. AC Turn-on / Dip Timing

8.8 PWOK_H SIGNAL

The PWOK_H is an open drain output with an internal pull-up to 3.3 V indicating whether both VSB and V1 outputs are within regulation. This pin is active-low. The timing diagram is shown in [Figure 26 / Figure 29](#) and referenced in the [Table 6](#).

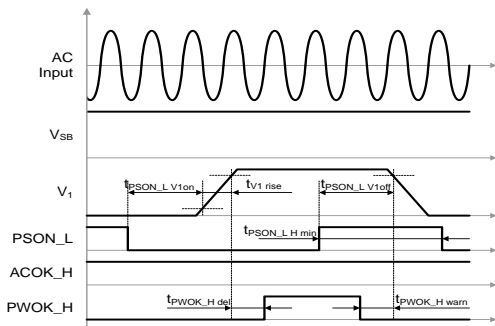


Figure 29. PSON_L turn-on/off timing

| OPERATING CONDITION | | MIN | MAX | UNIT |
|---------------------------|-------------------------------------|-----|-----|------|
| $t_{\text{PWOK_H del}}$ | PWOK_H to V1 delay (on) | 100 | 500 | ms |
| | PWOK_H to V1 delay (off) caused by: | | | |
| | PSKILL_H | 0 | 1 | ms |
| | PSON_L, ACOK_H, OT, Fan Failure | 1 | 2.5 | ms |
| $t_{\text{PWOK_H warn}}$ | UV and OV on VSB | 1 | 30 | ms |
| | OC on V1 (Software trigger) | -11 | 0 | ms |
| | OC on V1 (Hardware trigger) | -1 | 0 | ms |
| | OV on V1 | -3 | 0 | ms |

* A positive value means a warning time, a negative value a delay (after fact).

Table 4. PWOK_H timing

8.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the



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largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The standby output uses a passive current share method (droop output voltage characteristic).

8.10 SENSE INPUTS

Both main and standby outputs have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.

With open sense inputs the main output voltage will rise by 270 mV and the standby output by 50 mV. Therefore, if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN_H pin is high, the load current is low (see Figure 30) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I²C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE:

The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

Figure 33 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 45% is achievable.

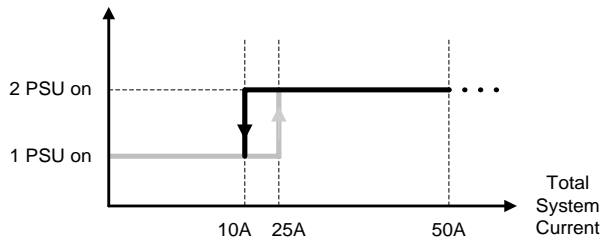


Figure 30. Hot-standby enable/disable current thresholds

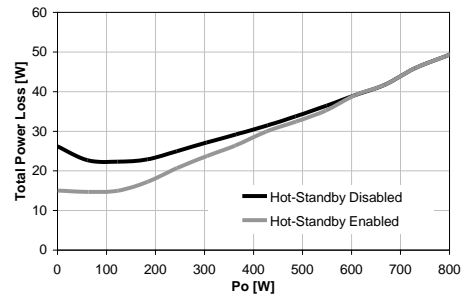


Figure 31. PSU power losses with/without hot-standby mode

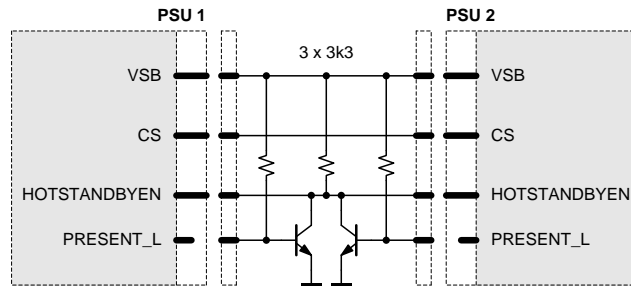


Figure 32. Recommended hot-standby configuration



In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure 32*. If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

8.12 I²C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the V1 Return. The PFE supply is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 7* further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

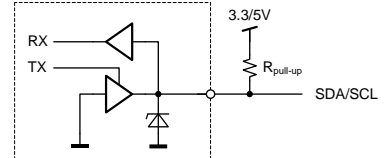


Figure 33. Physical layer of communication interface

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB_ALERT_L call address 25(0x19) by sending its status register. Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

| PARAMETER | DESCRIPTION | CONDITION | MIN | MAX | UNIT |
|--------------------|--|--|-----------------------------------|---------------------------------------|------|
| V _L | Input low voltage | | -0.5 | 1.0 | V |
| V _H | Input high voltage | | 2.3 | 5.5 | V |
| V _{hys} | Input hysteresis | | 0.15 | | V |
| V _{OL} | Output low voltage | 3 mA sink current | 0 | 0.4 | V |
| t _r | Rise time for SDA and SCL | | 20+0.1C _b ¹ | 300 | Ns |
| t _{of} | Output fall time V _{Hmin} → V _{Lmax} | 10 pF < C _b ¹ < 400 pF | 20+0.1C _b ¹ | 250 | Ns |
| I | Input current SCL/SDA | 0.1 VDD < V _i < 0.9 VDD | -10 | 10 | μA |
| C _i | Internal Capacitance for each SCL/SDA | | | 50 | pF |
| f _{SCL} | SCL clock frequency | | 0 | 100 | kHz |
| R _{pu} | External pull-up resistor | f _{SCL} ≤ 100 kHz | | 1000 ns / C _b ¹ | Ω |
| t _{HSTA} | Hold time (repeated) START | f _{SCL} ≤ 100 kHz | 4.0 | | μs |
| t _{LOW} | Low period of the SCL clock | f _{SCL} ≤ 100 kHz | 4.7 | | μs |
| t _{HIGH} | High period of the SCL clock | f _{SCL} ≤ 100 kHz | 4.0 | | μs |
| t _{SUSTA} | Setup time for a repeated START | f _{SCL} ≤ 100 kHz | 4.7 | | μs |
| t _{HDDAT} | Data hold time | f _{SCL} ≤ 100 kHz | 0 | 3.45 | μs |
| t _{SUDAT} | Data setup time | f _{SCL} ≤ 100 kHz | 250 | | ns |
| t _{SUSTO} | Setup time for STOP condition | f _{SCL} ≤ 100 kHz | 4.0 | | μs |
| t _{BUF} | Bus free time between STOP and START | f _{SCL} ≤ 100 kHz | 5 | | ms |

1 C_b = Capacitance of bus line in pF, typically in the range of 10...400 pF

Table 5. I²C / SMBus Specification



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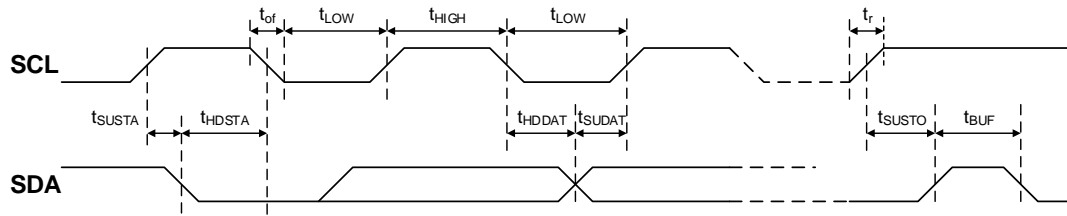


Figure 34. I²C / SMBus Timing

8.13 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the communication protocol and address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

NOTES:

If the APS pin is left open, the supply will operate with the PSMI protocol at controller / EEPROM addresses 0xB6/0xA6. The APS pin is only read at start-up of the power supply. Therefore, it is not possible to change the communication protocol and address dynamically.

| R _{APS} (Ω) ¹⁾ | Protocol | I ² C Address ²⁾ | |
|------------------------------------|----------------------|--|--------|
| | | Controller | EEPROM |
| 820 | Power Management Bus | 0xB0 | 0xA0 |
| 2700 | | 0xB2 | 0xA2 |
| 5600 | | 0xB4 | 0xA4 |
| 8200 | PSMI | 0xB6 | 0xA6 |
| 15000 | | 0xB0 | 0xA0 |
| 27000 | | 0xB2 | 0xA2 |
| 56000 | | 0xB4 | 0xA4 |
| 180000 | | 0xB6 | 0xA6 |

¹⁾ E12 resistor values, use max 5% resistors, see also Figure 35.

²⁾ The LSB of the address byte is the R/W bit.

Table 6. Address and protocol encoding

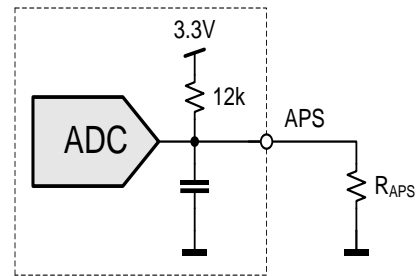


Figure 35. I²C address and protocol setting

8.14 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I²C bus physical layer (see Figure 36). An I²C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction. The DSP will automatically set the I²C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

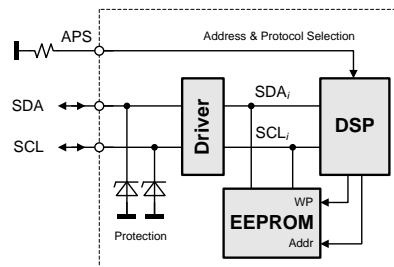


Figure 36. I²C Bus to DSP and EEPROM

8.15 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

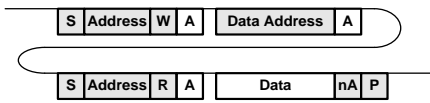
WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



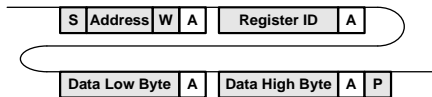
8.16 PSMI PROTOCOL

New power management features in computer systems require the system to communicate with the power supply to access current, voltage, fan speed, and temperature information. Current measurements provide data to the system for determining potential system configuration limitations and provide actual system power consumption for facility planning. Temperature and fan monitoring allow the system to better manage fan speeds and temperatures for optimizing system acoustics. Voltage monitoring allows the system to calculate input wattage and warning of system voltage regulation problems. The Power Supply Management Interface (PSMI) supports diagnostic capabilities and allows managing of redundant power supplies. The communication method is SMBus. The current design guideline is version 2.12.

The communication protocol is register based and defines a read and write communication protocol to read / write to a single register address. All registers are accessed via the same basic command given below. No PEC (Packet Error Code) is used.

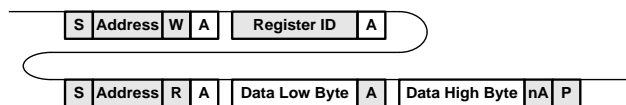
WRITE

The write protocol used is the SMBus 2.0 Write Word protocol. All writes are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device. See PFE Programming Manual for further information.



READ

The read protocol used is the SMBus 2.0 Read Word protocol. All reads are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device. See PFE Programming Manual for further information.



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8.17 POWER MANAGEMENT BUS PROTOCOL

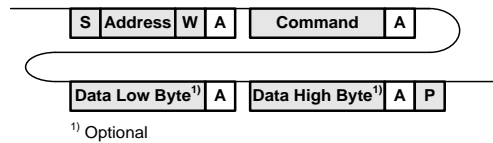
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PFE1100-12-054xA supply supports the following basic command structures:

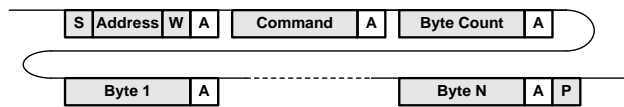
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

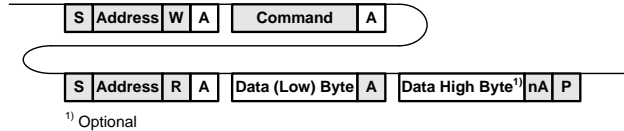


In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual for further information.

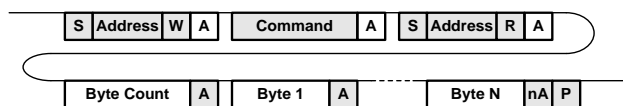


READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual BCA.00006 for further information.



8.18 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its “I²C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE1100-12-054xA Front-End.

The utility can be downloaded on belfuse.com/power-solution and supports both the PSMI and Power Management Bus protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

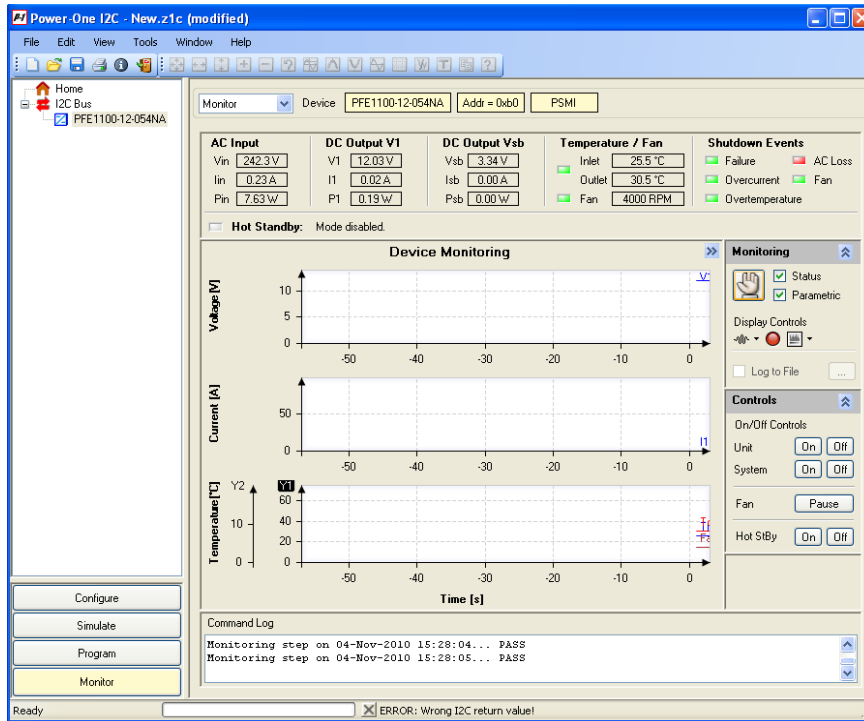
If the GUI is used in conjunction with the SNP-OP-BOARD-01 Evaluation Kit it is also possible to control the PSON_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (like the evaluation kit).

NOTE:

The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.



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9 TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE1100-12-054NA is provided with a normal airflow, which means the air enters through the rear of the supply and leaves at the front. The PFE1100-12-054RA is provided with a reverse airflow, which means the air enters through the front of the supply and leaves at the rear. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 105°C. If 70°C mating connector is used then end user must derate the input power to meet a maximum 70°C temperature at the front, see Figure 42.

NOTE:

It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

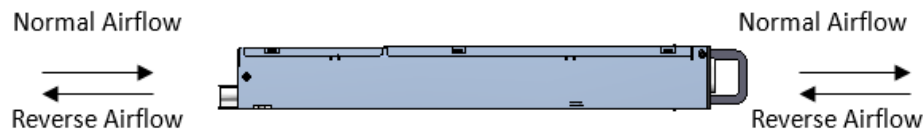


Figure 37. Airflow direction

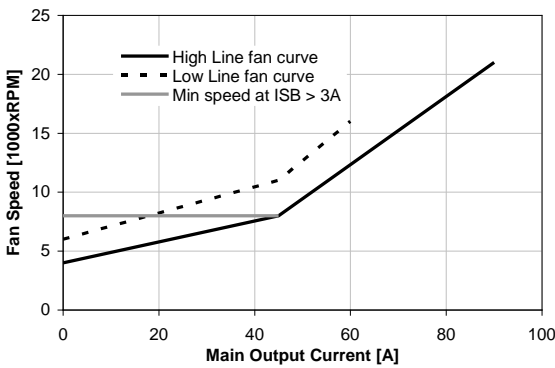


Figure 38. Fan speed vs. main output load for PFE1100-12-054NA

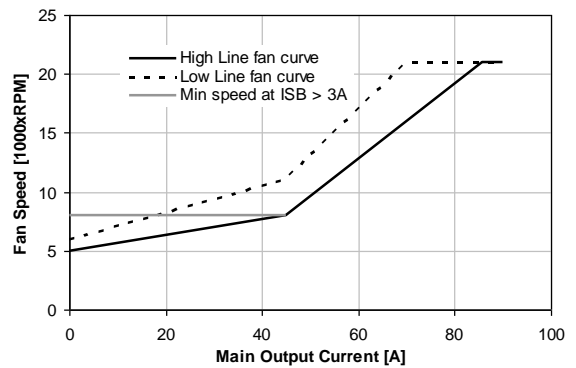


Figure 39. Fan speed vs. main output load for PFE1100-12-054RA

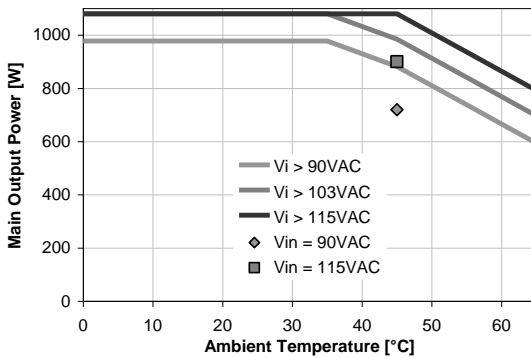


Figure 40. Thermal derating for PFE1100-12-054NA

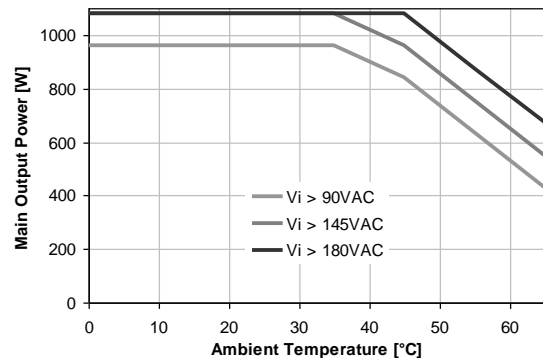


Figure 41. Thermal derating for PFE1100-12-054RA



10 ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

NOTE: Most of the immunity requirements are derived from EN 55024: 2010 + A1:2015.

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|--------------------------------|--|--|
| ESD Contact Discharge | IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body) | B |
| ESD Air Discharge | IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces) | B |
| Radiated Electromagnetic Field | IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz...2 GHz | A |
| Burst | IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute | B |
| Surge | IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV | V _{SB} : A; V _I : B ¹ A |
| RF Conducted Immunity | IEC/EN 61000-4-6, Level 3, 10 V _{rms} , CW, 0.1 ... 80 MHz | A |
| Voltage Dips and Interruptions | IEC/EN 61000-4-11 1: V _i 230 V, 100% Load, Phase 0°, Dip 100%, Duration 10 ms 2: V _i 230 V, 100% Load, Phase 0°, Dip 100%, Duration 20 ms 3: V _i 230 V, 100% Load, Phase 0°, Dip 100%, Duration >20 ms | A V _{SB} : A; V _I : B V _{SB} , V _I : B |

10.2 EMISSION

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|--------------------|--|------------------------|
| Conducted Emission | EN 55032 / CISPR 22: 0.15 ... 30 MHz, QP and AVG, single unit | Class A 6 dB margin |
| | EN 55032 / CISPR 22: 0.15 ... 30 MHz, QP and AVG, 2 units in rack system | Class A 6 dB margin |
| Radiated Emission | EN 55032 / CISPR 22: 30 MHz ... 1 GHz, QP, single unit | Class A 6 dB margin |
| | EN 55032 / CISPR 22: 30 MHz ... 1 GHz, QP, 2 units in rack system | Class A 6 dB margin |
| Harmonic Emissions | IEC 61000-3-2, V _{in} = 115 VAC / 60 Hz, & V _{in} = 230VAC/ 50 Hz, 100% Load | Class A |
| Acoustical Noise | 46 dBA at 1 meter, 25°C, 50% Load | - |
| AC Flicker | IEC 61000-3-3, V _{in} = 230 VAC / 60 Hz, 100% Load | Pass |

11 SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to EN/IEC 62368-1, and UL/CSA 62368-1.

Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--------------------------|---|--------------|-----|-----------------------------------|------------|
| Agency Approvals | Approved to latest edition of the following standards: UL/CSA 62368-1 and EN/IEC 62368-1 | | | | |
| Isolation Strength | Input (L/N) to case (PE) Input (L/N) to output Output to case (PE) | | | Basic Reinforced Functional | |
| ⊘ Creepage / Clearance | Primary (L/N) to protective earth (PE) Primary to secondary | | | | |
| Electrical Strength Test | Input to case Input to output (tested by manufacturer only) | 2500 4000 | | | VDC VDC |



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12 ENVIROMENTAL

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---------------------|-------------------------|---|-----|--------|------|
| T_A | Ambient Temperature | $V_{i \min}$ to $V_{i \max}$, $I_{o \text{ nom}}$, $I_{sB \text{ nom}}$ | | +45 | °C |
| $T_{A \text{ ext}}$ | Extended Temp. Range | | | +65 | °C |
| T_S | Storage Temperature | | | +70 | °C |
| | Altitude | | | 10,000 | Feet |
| N_a | Audible Noise | $V_{i \text{ nom}}$, 50% $I_{o \text{ nom}}$, $T_A = 25^\circ\text{C}$ | | 42 | dBA |

13 MECHANICAL

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|-----------|-------------------------|-----|-------|-----|------|
| | Dimensions | | 54.5 | | mm |
| | Height | | 40.0 | | |
| | Depth | | 321.5 | | |
| M | Weight | | 1050 | | g |

NOTE: A 3D step file of the power supply casing is available on request.

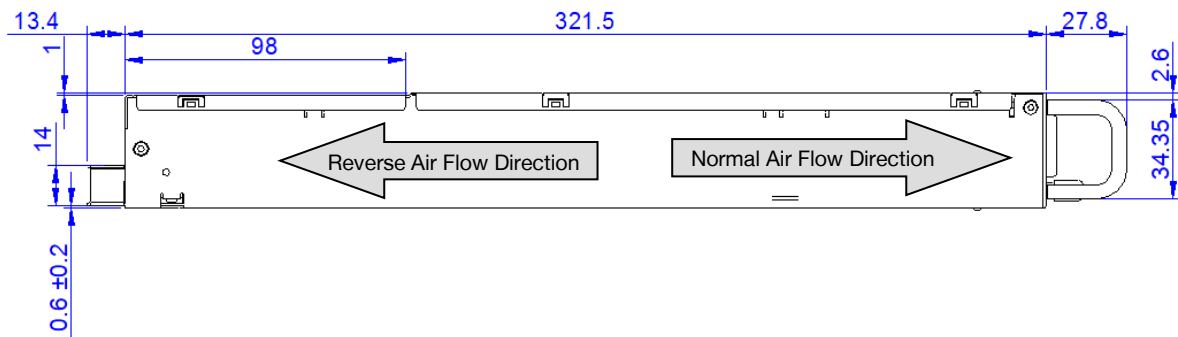


Figure 42. Side View 1

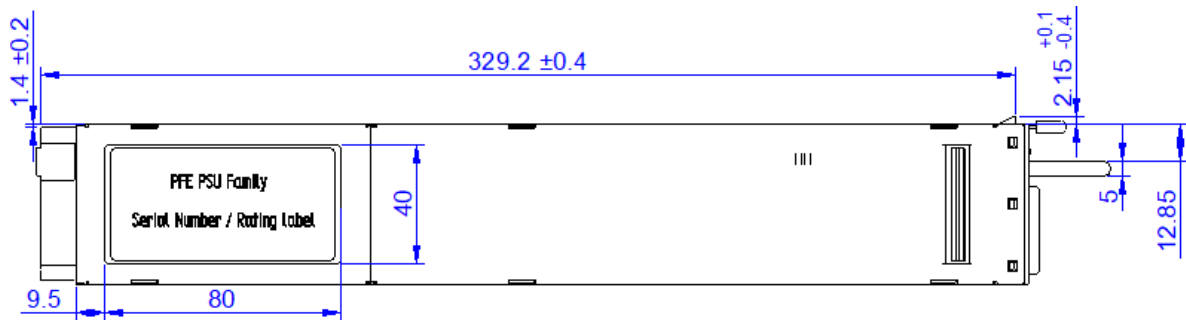


Figure 43. Top View



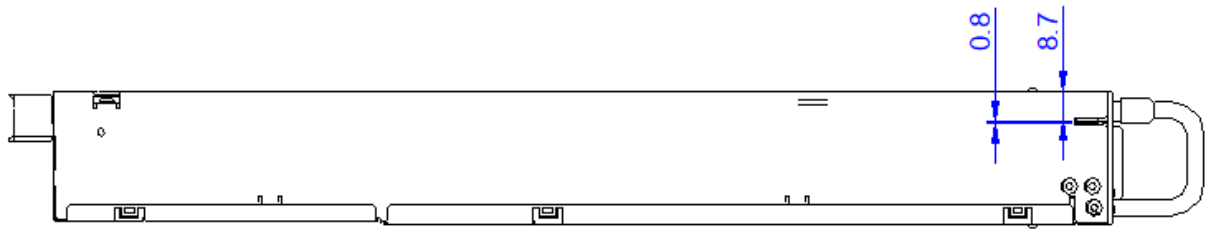


Figure 44. Side View 2

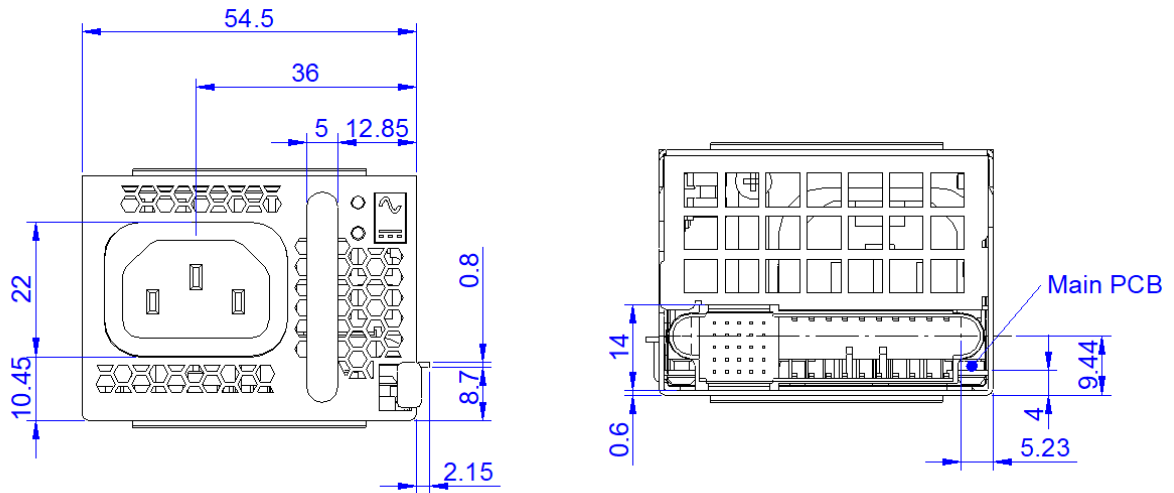


Figure 45. Front and Rear View



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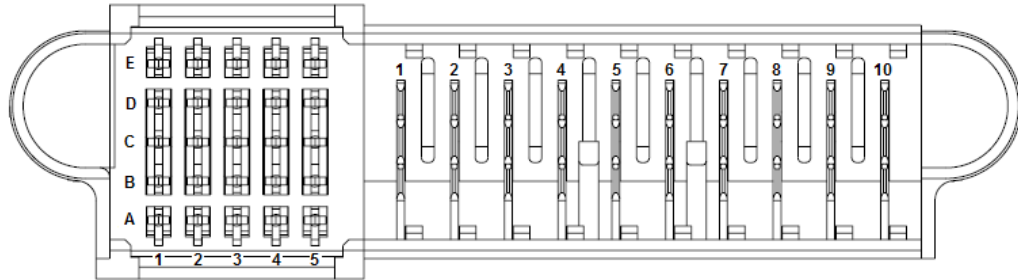
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14 CONNECTIONS





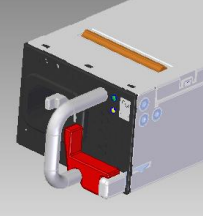
Power Supply Connector: Tyco Electronics P/N 1926736-3 or FCI connector 10133129-002LF or equivalent
(NOTE: Column 5 is recessed (short pins))

Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

| PIN | NAME | DESCRIPTION |
|---------------------|----------------|--|
| <i>Output</i> | | |
| 6, 7, 8, 9, 10 | V1 | +12 VDC main output |
| 1, 2, 3, 4, 5 | PGND | Power ground (return) |
| <i>Control Pins</i> | | |
| A1 | VSB | Standby positive output (+3.3/5 V) |
| B1 | VSB | Standby positive output (+3.3/5 V) |
| C1 | VSB | Standby positive output (+3.3/5 V) |
| D1 | VSB | Standby positive output (+3.3/5 V) |
| E1 | VSB | Standby positive output (+3.3/5 V) |
| A2 | SGND | Signal ground (return) |
| B2 | SGND | Signal ground (return) |
| C2 | HOTSTANDBYEN_H | Hot standby enable signal: active-high |
| D2 | VSB_SENSE_R | Standby output negative sense |
| E2 | VSB_SENSE | Standby output positive sense |
| A3 | APS | I ² C address and protocol selection (select by a pull down resistor) |
| B3 | N/C | Reserved |
| C3 | SDA | I ² C data signal line |
| D3 | V1_SENSE_R | Main output negative sense |
| E3 | V1_SENSE | Main output positive sense |
| A4 | SCL | I ² C clock signal line |
| B4 | PSON_L | Power supply on input (connect to A2/B2 to turn unit on): active-low |
| C4 | SMB_ALERT_L | SMB Alert signal output: active-low |
| D4 | N/C | Reserved |
| E4 | ACOK_H | AC input OK signal: active-high |
| A5 | PSKILL_H | Power supply kill (lagging pin): active-high |
| B5 | ISHARE | Current share bus (lagging pin) |
| C5 | PWOK_H | Power OK signal output (lagging pin): active-high |
| D5 | VSB_SEL | Standby voltage selection (lagging pin) |
| E5 | PRESENT_L | Power supply present (lagging pin): active-low |



15 ACCESSORIES

| ITEM | DESCRIPTION | ORDERING PART NUMBER | SOURCE |
|---|---|----------------------|--|
|  | <p>I²C Utility Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units)</p> | N/A | belfuse.com/power-solution |
|  | <p>Dual Connector Board Connector board to operate 2 PFE units in parallel. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).</p> | SNP-OP-BOARD-01 | Bel Power Solution |
|  | <p>Latch Lock Optional latch lock to prevent accidental removal of the power supply from the system while the AC plug is engaged.</p> | XSL.00019.0 | Bel Power Solution |

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



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